What is claimed is:

1. A display driver which drives a plurality of data lines of an electro-optical device which includes a plurality of pixels, a plurality of scan lines, and the data lines, the display driver comprising:

a gray-scale bus to which gray-scale data is supplied;

a capture start timing setting register in which is set a period between a changing time of a given capture start timing instruction signal and a staring time of capturing the gray-scale data;

a shift start signal generation circuit which generates a shift start signal based on a setting state of the capture start timing setting register;

a shift register which includes a plurality of flip-flops, shifts the shift start signal based on a given shift clock signal, and outputs a shift output from each of the flip-flops;

a data latch which includes a plurality of flip-flops, each of which holds the gray-scale data on the gray-scale bus based on the shift output from the shift register; and

a data line driver circuit which outputs a data signal corresponding to the gray-scale data held in the data latch to the data lines.

2. A display driver which drives a plurality of data signal supply lines of an electro-optical device which includes a plurality of pixels, a plurality of scan lines, a plurality of data lines, the data signal supply lines, and a plurality of demultiplexers, the data lines including data line groups alternately distributed inward from two opposite sides of the electro-optical device in a shape of comb teeth, each of the data line groups consisting of 3×N numbers of the data lines (N is a natural number), each of the data signal supply lines transmitting multiplexed data in which N set of data signals for first

to third color components is multiplexed, and each of the demultiplexers demultiplexing the multiplexed data and outputting one of the data signals for the first to third color components to each of the 3×N data lines, the display driver comprising:

a gray-scale bus to which gray-scale data for one of the first to third color components is supplied corresponding to an arrangement order of each of the data lines;

N first clock signal line being provided with one of 2×N shift clock signals and belonging to one of first to N-th groups;

N second clock signal line being provided with one of the 2×N shift clock signals and belonging to one of the first to N-th groups;

a capture start timing setting register in which is set a period between a changing time of a given capture start timing instruction signal and a staring time of capturing the gray-scale data;

a shift start signal generation circuit which generates a shift start signal based on a setting state of the capture start timing setting register;

a shift clock signal assignment circuit which assigns and outputs each of the 2×N shift clock signals to one of the first clock signal lines and one of the second clock signal lines based on a setting state of the capture start timing setting register;

N first shift register including a plurality of flip-flops, shifting the shift start signal in a first shift direction based on one of the shift clock signals, outputting a shift output from each of the flip-flops, and belonging to one of the first to N-th groups;

N second shift register including a plurality of flip-flops, shifting the shift start signal in a second shift direction opposite to the first direction based on one of the shift clock signals, outputting a shift output from each of the flip-flops in the second shift register, and belonging to one of the first to N-th groups;

N first data latch holding the gray-scale data on the gray-scale bus based on the shift output from the first shift register and belonging to one of the first to N-th groups;

N second data latch holding the gray-scale data on the gray-scale bus based on

the shift output from the second shift register and belonging to one of the first to N-th groups;

a multiplexer which generates first multiplexed data in which N set of the gray-scale data held in the first data latch is multiplexed and second multiplexed data in which N set of the gray-scale data held in the second data latch is multiplexed; and

a data-signal-supply-line driver circuit in which a plurality of data output sections are disposed corresponding to the arrangement order of each of the data lines, each of the data output sections outputting a data signal corresponding to the first or second multiplexed data to one of the data signal supply lines,

wherein the first shift register belonging to a j-th group ($1 \leq j \leq N$, j is an integer) among the first to N-th groups outputs the shift output based on one of the shift clock signals on the first clock signal line belonging to the j-th group,

wherein the second shift register belonging to the j-th group outputs the shift output based on one of the shift clock signals on the second clock signal line belonging to the j-th group,

wherein the first data latch belonging to the j-th group holds the gray-scale data based on the shift output from the first shift register belonging to the j-th group, and

wherein the second data latch belonging to the j-th group holds the gray-scale data based on the shift output from the second shift register belonging to the j-th group.

3. The display driver as defined in claim 2, comprising:

a line latch which latches N set of the gray-scale data held in the first data latch and N set of the gray-scale data held in the second data latch,

wherein the multiplexer generates the first multiplexed data in which the N set of gray-scale data from the first data latch among the gray-scale data held in the line latch is multiplexed, and generates the second multiplexed data in which the N set of gray-scale data from the second data latch among the gray-scale data held in the line

latch is multiplexed.

4. The display driver as defined in claim 2,

wherein the data-signal-supply-line driver circuit drives the data signal supply lines from a first side of the electro-optical device based on the first multiplexed data, and drives the data signal supply lines from a second side of the electro-optical device based on the second multiplexed data, the second side being opposite to the first side.

5. The display driver as defined in claim3,

wherein the data-signal-supply-line driver circuit drives the data signal supply lines from a first side of the electro-optical device based on the first multiplexed data, and drives the data signal supply lines from a second side of the electro-optical device based on the second multiplexed data, the second side being opposite to the first side.

6. The display driver as defined in claim 2, comprising:

a shift clock signal generation circuit which generates the 2×N shift clock signals based on a given reference clock signal,

wherein the gray-scale data is supplied to the gray-scale bus in synchronization with the reference clock signal, and

wherein the 2×N shift clock signals include a period in which the shift clock signals differ in phase.

7. The display driver as defined in claim 3, comprising:

a shift clock signal generation circuit which generates the 2×N shift clock signals based on a given reference clock signal,

wherein the gray-scale data is supplied to the gray-scale bus in synchronization with the reference clock signal, and

wherein the 2×N shift clock signals include a period in which the shift clock signals differ in phase.

8. The display driver as defined in claim 4, comprising:

a shift clock signal generation circuit which generates the 2×N shift clock signals based on a given reference clock signal,

wherein the gray-scale data is supplied to the gray-scale bus in synchronization with the reference clock signal, and

wherein the 2×N shift clock signals include a period in which the shift clock signals differ in phase.

9. The display driver as defined in claim 6,

wherein the 2×N shift clock signals include a given pulse in a first stage capture period for capturing the shift start signal in each of the first and second shift registers, and differ in phase in a data capture period after the first stage capture period has elapsed.

10. The display driver as defined in claim 7,

wherein the 2×N shift clock signals include a given pulse in a first stage capture period for capturing the shift start signal in each of the first and second shift registers, and differ in phase in a data capture period after the first stage capture period has elapsed.

11. The display driver as defined in claim 8,

wherein the 2×N shift clock signals include a given pulse in a first stage capture period for capturing the shift start signal in each of the first and second shift registers, and differ in phase in a data capture period after the first stage capture period has

elapsed.

12. The display driver as defined in claim 2,

wherein the shift clock signal assignment circuit outputs the 2×N shift clock signals to one of the N first clock signal line and the N second clock signal line corresponding to number of a given reference clock signal between the changing time of the capture start timing instruction signal and the staring time of capturing the gray-scale data.

13. The display driver as defined in claim 3,

wherein the shift clock signal assignment circuit outputs the 2×N shift clock signals to one of the N first clock signal line and the N second clock signal line corresponding to number of a given reference clock signal between the changing time of the capture start timing instruction signal and the staring time of capturing the gray-scale data.

14. The display driver as defined in claim 4,

wherein the shift clock signal assignment circuit outputs the 2×N shift clock signals to one of the N first clock signal line and the N second clock signal line corresponding to number of a given reference clock signal between the changing time of the capture start timing instruction signal and the staring time of capturing the gray-scale data.

15. The display driver as defined in claim 5,

wherein the shift clock signal assignment circuit outputs the 2×N shift clock signals to one of the N first clock signal line and the N second clock signal line corresponding to number of a given reference clock signal between the changing time of

the capture start timing instruction signal and the staring time of capturing the gray-scale data.

16 The display driver as defined in claim 6,

wherein the shift clock signal assignment circuit outputs the 2×N shift clock signals to one of the N first clock signal line and the N second clock signal line corresponding to number of a given reference clock signal between the changing time of the capture start timing instruction signal and the staring time of capturing the gray-scale data.

17. The display driver as defined in claim 7,

wherein the shift clock signal assignment circuit outputs the 2×N shift clock signals to one of the N first clock signal line and the N second clock signal line corresponding to number of a given reference clock signal between the changing time of the capture start timing instruction signal and the staring time of capturing the gray-scale data.

18. The display driver as defined in claim 8,

wherein the shift clock signal assignment circuit outputs the 2×N shift clock signals to one of the N first clock signal line and the N second clock signal line corresponding to number of a given reference clock signal between the changing time of the capture start timing instruction signal and the staring time of capturing the gray-scale data.

19. The display driver as defined in claim 9,

wherein the shift clock signal assignment circuit outputs the 2×N shift clock signals to one of the N first clock signal line and the N second clock signal line

corresponding to number of a given reference clock signal between the changing time of the capture start timing instruction signal and the staring time of capturing the gray-scale data.

20. The display driver as defined in claim 10,

wherein the shift clock signal assignment circuit outputs the 2×N shift clock signals to one of the N first clock signal line and the N second clock signal line corresponding to number of a given reference clock signal between the changing time of the capture start timing instruction signal and the staring time of capturing the gray-scale data.

21. The display driver as defined in claim 11,

wherein the shift clock signal assignment circuit outputs the 2×N shift clock signals to one of the N first clock signal line and the N second clock signal line corresponding to number of a given reference clock signal between the changing time of the capture start timing instruction signal and the staring time of capturing the gray-scale data.

22. The display driver as defined in claim 12,

wherein, when the number of the reference clock signal at a rising edge or a falling edge of the reference clock signal immediately after the changing time of the capture start timing instruction signal is "0", the shift clock signal assignment circuit outputs the 2×N shift clock signals to one of the N first clock signal line and the N second clock signal line depending on whether the number of the reference clock signal between the changing time of the capture start timing instruction signal and the starting time of capturing the gray-scale data is an even number or an odd number.

23. The display driver as defined in claim 13,

wherein, when the number of the reference clock signal at a rising edge or a falling edge of the reference clock signal immediately after the changing time of the capture start timing instruction signal is "0", the shift clock signal assignment circuit outputs the 2×N shift clock signals to one of the N first clock signal line and the N second clock signal line depending on whether the number of the reference clock signal between the changing time of the capture start timing instruction signal and the starting time of capturing the gray-scale data is an even number or an odd number.

24. The display driver as defined in claim 2,

wherein a direction from a first side to a second side of the electro-optical device in which the data lines extend is the same as one of the first and second shift directions, the second side being opposite to the first side.

25. The display driver as defined in claim 1,

wherein, when a direction in which the scan lines extend is a long side and a direction in which the data lines extend is a short side, the display driver is disposed along the short side of the electro-optical device.

26. The display driver as defined in claim 2,

wherein, when a direction in which the scan lines extend is a long side and a direction in which the data lines extend is a short side, the display driver is disposed along the short side of the electro-optical device.

27. An electro-optical device comprising:

a plurality of pixels;

a plurality of scan lines;

a plurality of data lines, the data lines including data line groups alternately distributed inward from two opposite sides of the electro-optical device in a shape of comb teeth, and each of the data line groups consisting of 3×N numbers of the data lines (N is a natural number);

a plurality of data signal supply lines, each of the data signal supply lines transmitting multiplexed data in which N set of data signals for first to third color components is multiplexed;

a plurality of demultiplexers, each of the demultiplexers demultiplexing the multiplexed data and outputting one of the data signals for the first to third color components to each of the 3×N data lines; and

the display driver as defined in claim 2 which drives the data signal supply lines.

28. An electro-optical device comprising:

a display panel including:

a plurality of pixels;

a plurality of scan lines;

a plurality of data lines, the data lines including data line groups alternately distributed inward from two opposite sides of the electro-optical device in a shape of comb teeth, and each of the data line groups consisting of 3×N numbers of the data lines (N is a natural number);

a plurality of data signal supply lines, each of the data signal supply lines transmitting multiplexed data in which N set of data signals for first to third color components is multiplexed; and

a plurality of demultiplexers, each of the demultiplexers demultiplexing the multiplexed data and outputting one of the data signals for the first to third color components to each of the 3×N data lines, and

the display driver as defined in claim 2 which drives the data signal supply lines.